IP3023™ Wireless Network Processor

250 MIPS 8-Way Multithreaded Processor Optimized for Network Connectivity

1.0 Product Highlights

The IP3023™ wireless network processor is a revolutionary new platform from Ubicom designed to provide highly integrated solutions for applications at the "edge" of Internet connectivity, including 802.11a/b/g access points, routers, hot spots, bridges, gateways, and a wide variety of embedded networked client solutions. The IP3023 is optimized for efficient network processing in embedded solutions. Its development has led to the definition of a new microprocessor architecture: MASI (Multithreaded Architecture for Software I/O). Many MASI concepts were pioneered in the Ubicom IP2000 family of processors, but the IP3023 dramatically extends those techniques by introducing hardware support for multiple threads operating with no context switching overhead, and three-operand memory-to-memory operations.

The IP3023 is a 250 MIPS 32-bit CPU supporting 8-way multithreaded operation. It provides for up to 8 real-time tasks to execute in a completely deterministic fashion. In essence, the IP3023 supports running a different thread on every clock, but without the overhead for context switching typical with traditional microprocessor architectures. To the system designer, the IP3023 appears as if there were 8 processors on the chip.

The multithreaded and deterministic nature of the IP3023 processor provides for integration of numerous functions on chip – some with on-chip hardware assist and some entirely in software – as threads, including the ability to support interfaces such as 10/100 MII and 10Base-T Ethernet MAC/PHY, USB, GPSI, Utopia, PCMCIA, IDE, PCM Highway, and CardBus/Mini PCI interface specific for 802.11a/g wireless

Key Features:

- 250 MIPS, 32-bit MASI CPU
- IP3023 is optimized for wireless networking
  - 8-way simultaneous multithreading
  - Deterministic execution on all threads
  - Zero overhead full context switching
  - Programmable MIPS per thread
  - Optimized ISA for packet processing
    - Memory to memory architecture, powerful addressing modes
    - Small fast instruction set, strong bit manipulation
    - Reduced code size vs RISC CPUs
- On-chip program and data memory
  - Eliminates cache miss penalties
  - 256 KB (64K x 32) of Program SRAM
  - 64 KB (16K x 32) of Data SRAM
- Highly configurable I/O support
  - Many Combinations of Software I/O:
    - Utopia, PCMCIA, IDE/ATAPI
    - PCM Highway, UART, SPI, I2C
    - 32-bit 802.11a/g radios interface
  - Two SerDes for fast serial I/O:
    - 10Base-T (MAC/PHY), USB, GPSI
    - SPI, UART, 2-wire serial, BlueRF
    - Up to 4 MII ports for 10/100 PHY
- Additional key hardware
  - True random number generator for software-implemented encryption/security (32-bit seed)
  - Fixed-point MAC (16x16+48-bit, 250 additional MOPS) for voice/audio codecs, other signal processing tasks
- Independent I/O and core CPU clocking
  - Separate Phase-Locked Loops (PLLs)
  - Programmable multipliers & dividers
  - Single low cost crystal (10MHz)

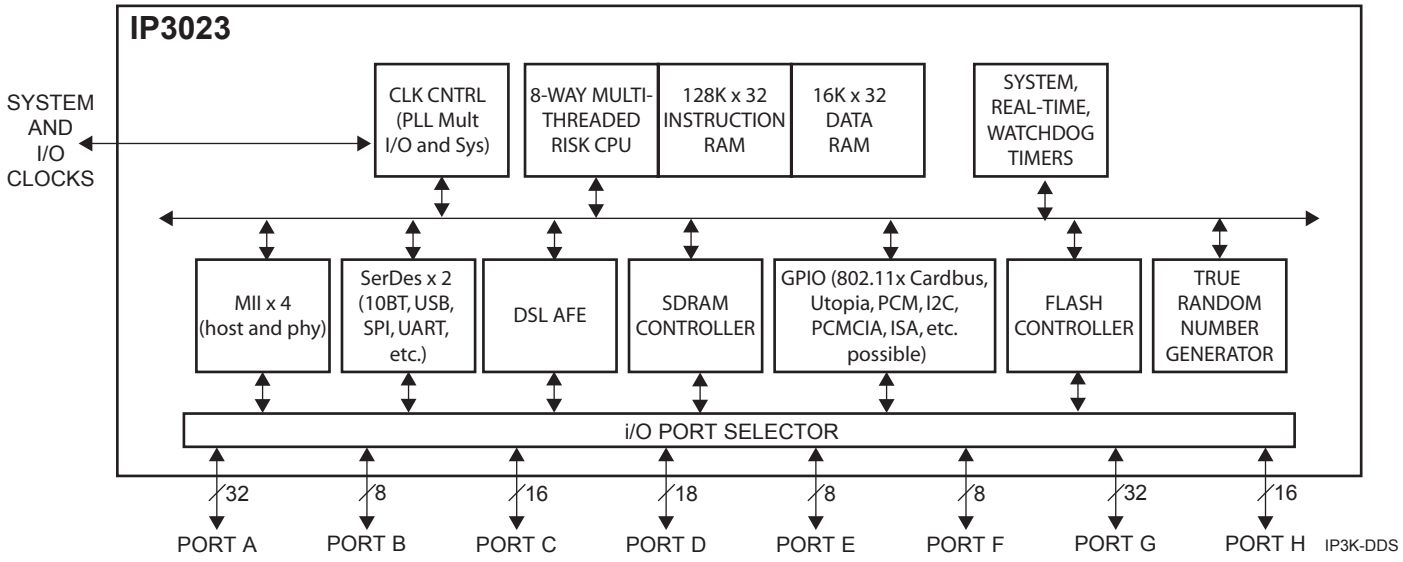

Figure 1-1 IP3023 Block Diagram

radios. This yields both a high degree of flexibility and reduces die size, as it eliminates the need for many on-chip dedicated hardware blocks for specific functions.

The IP3023 employs a three-operand memory-to-memory architecture, utilizing on-chip program and data memory support. This scheme enables highly efficient data movement and processing on data. The result is that the IP3023 is designed to support packet processing and transfers at wire speeds, eliminating the need for caches and large data buffers typically found in use with traditional RISC-based microprocessors.

To further optimize the IP3023 for networking infrastructure and embedded client solutions, the processor includes several key hardware support blocks, including true random number generator and fixed-point multiply/accumulate (MAC) units. The random number generator facilitates robust software implementation of common encryption/security protocols, critical to the continued growth of wireless networking. The MAC unit supports up to 500 MOPS for the whole IP3023, because it runs independently of the main pipeline, making it ideal for implementation of voice/audio codecs and other signal processing tasks.

1.1 Additional Features

IP3023 Wireless Network Processor Capabilities

Foundation for Highly Flexible Connectivity Solution

- 250 MHz internal clock; 250 MIPS performance.
- Additional 250 MMAC performance from fixed point 16x16x48 bit MAC unit.
- On-chip dual-ported SRAM data memory.
- On-chip SRAM program memory.
- On-chip hardware for zero overhead instruction level context switch for multithreading.
- In-system programming of external flash.

Multiple Networking Protocols and Physical Layer Support Hardware

- Two full-duplex serializer/deserializer (SerDes) channels.
  - Flexible to support 10Base-T, GPSI, SPI, UART, USB protocols, BlueRF.
  - One on-chip PHY function for 10Base-T Ethernet.
- Four MII Ports, each MII can operate in host or phy mode.

Memory

- 256 KB (64K x 33) on-chip program SRAM with 1-bit parity.
- 64 KB (16K x 32) on-chip dual port data SRAM.
- Up to 4 MB (4M x 8) off-chip Flash support.
- Up to 64 MB (32M x 16) off-chip PC 66/100/133 SDRAM support.

IP3023 Wireless Network Processor Features

- 32-bit data and instruction paths (fixed instruction width).
- All instructions execute in one clock cycle.
- 8-way instruction level multithreading with support for both hard and non-real-time thread priority scheduling.
- Multiply and multiply/accumulate instructions, where MAC uses a 48-bit accumulator.
- Special purpose CRC instruction for CRC generation/checking and encryption.
- 8 x 16 general-purpose 32-bit registers.
- 8 x 8 32-bit address registers.
- Linear address space.
- High instruction code density.

General-Purpose Hardware Peripherals

- True random number generator (32-bit seed number).
- One 32-bit system timer synchronous with system clock with 8 compare registers.
- One 32-bit real-time counter with constant clock frequency.
- Watchdog 32-bit timer with constant clock frequency.
- Power-on reset circuit.
- Brownout minimum supply voltage detector.
- 8 external interrupt inputs mapped to I/O ports.
- Two programmable output clocks.

Sophisticated Power and Frequency/Clock Management Support

- Operating voltage from 1.14V to 1.26V.
- Single clock input with 10–20 MHz oscillator and external clock input support.
- Two on-chip PLLs: one for processor clock, one for peripheral logic.
- Core clock using a selectable on chip divider.
- Software CPU speed control for power saving.
- Power-On-Reset (POR) and brownout logic.

Flexible I/O

- 136 I/O pins in 208-pin QFP option.
- 8 configurable multifunction I/O ports.
- 2.3V to 3.6V symmetric CMOS output drive.
- 5V-tolerant inputs.

Support for In-System Debug and Configuration

- Customer application program updatable.
  - Run-time self-programming.
- On-chip in-system debugging support interface.
- Debugging at full IP3023 operating speed.
- Real-time emulation, program debugging, and integrated software development environment offered by leading third-party tool vendors.

Complete Software Development Environment

IP3023 wireless network processor is capable of supporting the following functions in software. See a Ubicom sales representative for actual availability and schedule.

- ipOS™ operating system
- ipStack™ software
  - TCP/IP protocol stack (includes DNS, DHCP, SNMP, NAT, Firewall).
- ipWeb™ software – HTTP 1.1 Server
- ipFile™ flash virtual file system
- ipIO™ software – device I/O-driven interfaces
  - MII, Utopia I, 802.11x Cardbus, I^2C, SPI, GPSI, UART, BlueRF, PCM Highway.
  - 802.11a/b/g chipset drivers.
- ipModule™ software – pre-built connectivity software modules
  - ipEthernet™ module – 10Base-T Ethernet
  - ipHomePlug™ module– HomePlug® power line networking
  - ipUSBDevice™ module – USB 1.1 host or device
  - ipBlue™ module – Bluetooth
  - ipWLANStation™ module – 802.11a/b/g station (node or bridge)
  - ipWLANAccessPoint™ – 802.11a/b/g access point
- Configuration tool
  - Integrated tool to support rapid development efforts

Red Hat® GNUPro® tools including GCC ANSI C compiler and assembler, linker, utilities, and GNU debugger

Ubicom's Unity™ IDE including editor, project manager, graphical user interface to GNU debugger, device programmer, and ipModule configuration tool

1.2 I/O Port Mapping

IP3023 has very configurable port mapping. Port A for example supports the external Flash, but can also be shared with the SDRAM controller, and a PCMCIA interface when combined with Port B. Some of the ports share a dedicated HW function. Port E for example shares a part of an MII port, one of the on-board SerDes units, or part of a Utopia bus implementation in software. All ports can be used as GPIO ports. GPIO ports are used to create virtual I/O ports to control UTOPIA, 802.11a/b/g, PCM Highway, and other popular interfaces. Table 1-1 shows how the IP3023 I/O ports are shared, and shows possible I/O port mappings for three different applications.

1.3 Architecture

1.3.1 CPU

The CPU is a general-purpose 32-bit pipelined processor. The CPU implements multithreading in hardware and supports the execution of deterministic hard real-time (HRT) threads. Up to eight simultaneous threads are supported in hardware. Attached to the core are a 256KB instruction SRAM and a 64 KB data SRAM. The core also has access to an off-chip flash memory for code storage and booting. Code for the processing core is written in C as well as in assembly language.

1.3.2 CPU Instruction Memory

The instruction memory for the main processor is implemented as a single-port (256 KB with parity, 64K x 32) SRAM. This RAM is able to supply the main processor with one instruction access per clock and has a 2 clock read latency.

Table 1-1 I/O Ports and Example Configurations

I/O Port	Port Width	Actual Hardware I/O Support	ADSL Gateway	Home router	Wireless AP
Port A	32 bits	Flash	Flash	Flash	Flash
Port B	8 bits	SDRAM	SDRAM+WiFi	SDRAM+WiFi	SDRAM + WiFi
Port C	16 bits	MII	Utopia or AFE	MII	MII
Port D	18 bits	MII	MII	MII	MII
Port E	8 bits	SerDes or MII (1/2)	Utopia (GPIO with Port C) or USB	SerDes USB	SerDes BlueRF
Port F	8 bits	SerDes or MII (1/2)	PCM	SerDes Ethernet	GPIO (LED control)
Port G	32 bits	GPIO	802.11(a,g)	PCM	802.11(a,g)
Port H	16 bits	MII	802.11(a,g)	MII	802.11(a,g)

1.3.3 CPU Data Memory

The data memory for the main processor is 64 KB (16K x 32) SRAM. It is able to perform one read and one write per clock, in support of the three operand, memory-to-memory instruction set architecture. While the read and write bandwidth of this memory is one each per clock, data memory accesses are pipelined in the main processor pipe, and take two clocks to execute.

1.3.4 I/O Ports

1.3.5 Clocks, Frequency, and Timers

A single clock input (crystal, 10–20 MHz) is used to source multiple subsystems and peripherals in the IP3023. This clock source is fed into independent PLLs for generating a system clock and an I/O clock. Alternatively, the PLLs can be bypassed, and the 10-20 MHz clock input can be used directly. The PLLs are capable of generating up to a 250 MHz clock from the 10-20 MHz input signal.

This initial 10–20 MHz input is also fed into a real-time clock (RTC) timer, which can be used to maintain an accurate time base in a system.

1.3.6 Low Power Operation

Being fabricated in advanced process geometries and operating off a 1.2V supply, the IP3023 is inherently efficient in terms of low power operation. However, the IP3023 can also be configured for additional levels of power savings, based on varying the frequency of operation and clock source. These lower power modes can be used in combination with one another, and include:

1. Reducing the clock frequency out of the system clock PLL. – The clock circuit of the IP3023 includes a run-time controllable post-divider on the PLL output, allowing the developer to drop the operating frequency in steps down to 1/16 of the maximum operating frequency (i.e. 250 MHz full active frequency can be reduced down to as little as 15.625 MHz).
2. Reducing the clock frequency out of the I/O clock PLL. – As with the system clock PLL, the I/O clock PLL includes a run-time controllable post-divider at the output, allowing for I/O clock frequency reduction on the fly in steps down to 1/16 of the maximum operating frequency.
3. Turning off system clock PLL. – System clocking runs directly from the 10–20 MHz clock input.
4. Turning off I/O clock PLL. – I/O clocking runs directly from the 10–20 MHz clock input.

1.3.7 Interrupts

Flexible interrupts structure. Real-time interrupts can be handled by a traditional interrupt service routine (ISR) or individually assigned to independent threads.

1.3.8 Reset

The following sources are capable of causing a chip reset:

- Power-on
- Debug port
- Brownout
- Watchdog timer
- Parity Error
- External reset

1.3.9 Programming and Debugging

The IP3023 device has advanced in-system programming and debug support on-chip. This unobtrusive capability is provided through an ISP/ISD interface. There is no need for a bond-out chip for software development. This eliminates concerns about differences in electrical characteristics between a bond-out chip and the actual chip used in the target application. Designers can test and revise code on the same part used in the actual application.

Ubicom provides the complete Red Hat GNUPro tools, including C compiler, assembler, linker, utilities and GNU debugger. In addition, Ubicom offers an integrated graphical development environment which includes an editor, project manager, graphical user interface for the GNU debugger, device programmer, and ipModule™ configuration tool.

1.3.10 Other Supported Functions

- *Random number generator* – the IP3023 includes an on-chip hardware true random number generator. On-chip random noise generates random bits which are accumulated in a hardware 32-bit Linear Feedback Shift Register (LFSR). This function can be used to seed a software random number generator or to generate per-session cryptography keys.
- *Boot through debug port from external flash* – unlike the IP2000 family processors, there is no on-chip flash.

Sales and Technical Support Contact Information

For the latest contact and support information on IP devices, please visit the Ubicom Web site at www.ubicom.com. The site contains technical literature, local sales contacts, tech support, and many other features.

The Products are not authorized for use in life support systems or under conditions where failure of the Product would endanger the life or safety of the user, except when prior written approval is obtained from Ubicom, Inc. Ask your sales representive for details.

UBICOM™

635 Clyde Avenue
Mountain View, CA 94043

Tel: 650.210.1500
Fax: 650.210.8715
Email: sales@ubicom.com
Web: www.ubicom.com

Ubicom, Inc. develops and markets wireless network processor and software platforms that enable all electronic devices to be connected to each other – securely, cost-effectively and transparently. With headquarters in Mountain View, California, Ubicom also has offices in Southern California as well as Belgium, Taiwan and Hong Kong. For more information, visit www.ubicom.com.

IP3K-DTB-3023-10 (4/17/2003)